Abstract of the Disclosure

Disclosed is a semiconductor device capable of reducing parasitic capacitance and a method thereof, the method including the steps of depositing sequentially an inorganic silicon oxide layer and a low dielectric constant organic silicon oxide layer on a substrate, forming a partial trench with a predetermined depth in the organic silicon oxide layer by patterning, oxygenating an inner wall of the partial trench, and forming a trench by etching the partial trench with hydrofluoric acid (HF).